IN THE CLAIMS

Kindly amend claim 1 as shown in the attached claim listing:

1. (currently amended) A trench-gate semiconductor device, comprising:

a semiconductor body having an active cell area wherein physically connected trenches in an orthogonal pattern containing gate material extend into the semiconductor body from a surface thereof, wherein adjacent to each trench-gate there is a source region at said semiconductor body surface separated from a drain region by a channel-accommodating body region, and wherein a source electrode contacts the source regions on said semiconductor body surface;

the active cell area has a network of connected said trenches with a said source region in each said cell;

trenches containing gate material extend from the network of connected trenches beyond the active cell area to an inactive area where said source regions are not present;

within said inactive area there is a gate electrode contact area where a gate electrode contacts the gate material on the whole area of the trenches adjacent the semiconductor body surface and where the gate electrode also contacts the semiconductor body surface adjacent the trenches, wherein the semiconductor body surface contacted by the gate electrode has a first region at the

semiconductor body surface of one conductivity type, said first region having an underlying second region of opposite conductivity type; and

linking cells across the inactive and active areas, wherein each linking cell has a first region contacted by the gate electrode and a source region contacted by the source electrode, and wherein the underlying second region extends to the semiconductor body surface at an area between the source region of each linking cell and the first region of the linking cell, at which area the underlying second region is contacted by the source electrode.

2. (canceled).

3. (previously presented) A semiconductor device as claimed in claim 1, wherein the source regions in the active cell area and said first regions in the inactive area are of a same first conductivity type, wherein the channel-accommodating body regions in the active cell area and said second regions in the inactive area are of a same second conductivity type opposite to the first conductivity type, and wherein a common layer of the first conductivity type provides the drain regions in the active cell area and underlies the second regions in the inactive area.

4. (Original) A semiconductor device as claimed in claim 3, wherein said first regions and said underlying second regions in the inactive area are provided as isolated cells surrounded by a further network of connected trenches which is an extension of the network of connected trenches in the active cell area.

5. (previously presented) A semiconductor device as claimed in claim 4, modified in that at least some of said isolated cells in the inactive area which are nearest to the active area comprise the linking cells across the inactive and active areas, wherein each linking cell further includes the underlying second region continuous with a said channel-accommodating body region which extends to the semiconductor body surface where it is contacted by the source electrode, the linking cells providing voltage protection diodes between the gate electrode and the source electrode.

6. (previously presented) A semiconductor device as claimed in claim 3, wherein said trenches which extend from the network of connected trenches in the active cell area are stripe shaped trenches which each extend completely across the gate electrode contact area, wherein the linking cells are provided across the inactive and active areas between the stripe shaped trenches, wherein each linking cell further includes the underlying second

region continuous with a said channel-accommodating body region which extends to the semiconductor body surface where it is contacted by the source electrode, the linking cells providing voltage protection diodes between the gate electrode and the source electrode.

7. (previously presented) A semiconductor device as claimed in any one of claim 1, wherein a patterned insulating layer is provided on the semiconductor body, wherein in the active cell area the insulating layer provides an insulating overlayer on the trench-gates and the insulating layer has windows where the source electrode contacts the source regions, and wherein in the inactive area a window in the insulating layer provides the gate electrode contact area.

8. (previously presented) A semiconductor device as claimed in claim 1, wherein in the active cell area an insulating layer is provided in the trenches between the gate material in the trenches and the semiconductor body adjacent the trenches.

9. (previously presented) A semiconductor device as claimed in claim 1, wherein the gate electrode provides a gate bond pad within the gate electrode contact area.